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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/603,927	06/27/2000	YASUTAKA NAKASHIBA	186709/99	3707

466 7590 01/25/2005

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EXAMINER	
TRAN, NHAN T	
ART UNIT	**PAPER NUMBER**
2615	

DATE MAILED: 01/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/603,927	NAKASHIBA, YASUTAKA	
	Examiner	Art Unit	
	Nhan T. Tran	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 June 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-16 have been considered but are moot in view of the new ground of rejection.

Drawings

2. Figures 12-15 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claims 8 & 10 are objected to because the claims recite the limitation "said plurality of light shielding films." There is insufficient antecedent basis for this limitation in the claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kimura (US 6,172,351) in view of Hokari et al (US 6,618,087).

Regarding claim 1, Kimura discloses a solid-state image pickup device (Fig. 2; col. 1, lines 6-10) comprising:

a photoelectric conversion part (12) on a semiconductor substrate (11), the photoelectric conversion part having a photoelectric conversion region (inherent pixels), a logic part (peripheral circuits, i.e., ADC and memory portion, signal processing portion, etc.) on the semiconductor substrate, the logic part including a plurality of transistors to manipulate an electrical signal produced from the photoelectric conversion part (see Figs. 1B, 2 & 6, col. 2, lines 51-66). Also disclosed is a light shielding layer (TAB tape 17 and black insulation film 61, Figs. 1B & 6) that covers the logic circuit part (see col. 4, lines 26-34 and col. 3, lines 13-19).

As clearly seen from Figs. 1B & 6, the image pickup portion 12 is located closer to the substrate 11 than the TAB tape 17 and black insulation film 61 in view of this high level layout of the chip package. However, Kimura fails to explicitly disclose **a detailed structure** of the

image pickup portion 12 that comprises a light shielding film *defining* a region of beam incidence on the photoelectric conversion region. Hokari teaches a detailed layout of an imaging arrays that comprises a plurality of photoelectric conversion region (91, Fig. 7), wherein each photoelectric conversion region is defined by an opening of a light shield film as shown in Figs. 8 & 9; col. 7, lines 56-65. The light shield film is formed to prevent invasion of a light beam from entering surrounding circuits so as malfunction of such circuits is avoided (see col. 8, lines 17-30).

Therefore, it would have been obvious to one of ordinary skill in the art to combine the teachings of Kimura and Hokari such that *each* photoelectric conversion region of the image pickup portion 12 in Kimura would be formed by an opening of light shield film layer which would be closer to the semiconductor substrate than the light shielding layer so as to prevent malfunction of surrounding circuits (i.e., transfer gates, vertical transfer arrays, etc.) possibly caused by light from being incident thereon.

It is noted that the solid-state image device in Hokari can be configured in CMOS circuit (Hokari, col. 10, lines 15-20).

Regarding claim 2, the combination of Kimura and Hokari would disclose that the light shielding film is located at an intermediate position between the light shielding layer and said photoelectric conversion region in the direction of beam incidence. See Kimura, Figs. 1B & 6 and Hokari, Figs. 7-13.

Regarding claim 3, the combination of Kimura and Hokari would also disclose the light shielding state made by the combined of light shielding film (Figs. 8-13 in Hokari) and the black insulation film (61, Fig. 6 in Kimura) being continuous in the boundary part between the photoelectric conversion part and the logic circuit part since such configuration is intended to cover all circuitry surrounding photodiode with a light shielding material as suggested by Hokari in col. 8, lines 17-30.

Regarding claim 4, see the analysis of claim 3.

Regarding claim 5, since the light shielding configuration is implemented in the manner of overlapping light shielding materials as suggested by Hokari in Figs. 8-13 and col. 8, lines 17-30, it would have been obvious to one of ordinary skill in the art to implement the same overlapping manner to all light shielded areas throughout the chip package so as to make the light shielding state continuous in any boundary part.

Regarding claim 6, Hokari discloses that light shielding film covers the photoelectric conversion part by combining a plurality of layers (Figs. 9-13; col. 8, lines 17-30 and col. 9, lines 36-46).

Regarding claim 7, see the analysis of claim 6.

Regarding claim 8, it is clear in Hokari that the plurality of light shielding films are provided so as to make the light shielding state continuous in their boundary parts (Figs. 9-13). Also see the analysis of claim 5.

Regarding claim 9, see the analyses of claims 5 & 8 and Figs. 9-13 in Hokari.

Regarding claim 10, see the analyses of claims 1, 5 & 8 and Figs. 7-13 in Hokari and Figs.2 & 6 in Kimura for a combination wherein the light shielding state would be continuous throughout the chip package except for the photodiode.

Regarding claim 11, since the light shielding film is made of a resin or even a stackup of color filters to have low light transparency such that its light shielding property is high (see Hokari, col. 9, lines 35-46).

Regarding claim 12, both Kimura and Hokari teach an image pickup portion and its peripheral circuits are implemented using MOS type transistors (see Kimura, col. 2, lines 57-66 and Hokari, col. 10, lines 15-20). Therefore, the manufacturing process of both image pickup portion and its peripheral portions including light shield film would be the same.

Regarding claim 13, see the analysis of claim 1.

Regarding claim 14, both Kimura and Hokari disclose the solid-state image pickup device as a MOS type sensor that may include a CMOS sensor (Kimura, col. 2, lines 57-66 and Hokari, col. 10, lines 15-20).

Regarding claim 15, see the analysis of claim 1. Furthermore, Kimura discloses an A/D conversion portion 13c and a signal processing portion 13d that are formed on the same substrate 11 with the image pickup portion 12 (see Kimura, Fig. 2; col. 2, lines 51-66).

Regarding claim 16, it is clear that the image pickup portion 12 inherently includes a photoelectric conversion region (pixels) generating an electrical charge in response to the light and a transistor circuit (MOS type transistors) producing the analog signal in response to the electrical charge (Kimura, col. 2, lines 51-66).

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nhan T. Tran whose telephone number is (703) 605-4246. The examiner can normally be reached on Monday - Thursday, 8:00am - 6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew B Christensen can be reached on (703) 308-9644. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NT.

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